Remarks

In the present response, claims 1-16, 18-19, 21-26, and 28-34 are presented for examination.

Claim Rejections: 35 USC § 102(b) & 103(a)

Claims 1, 13, 16 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,887,138 to Hagersten et al. in view of U.S. Pat. No. 6,185,658 B1 to Arimilli et al. Claims 2-5,7,8,14,15,18,19,21,22,25,26,28,29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,887,138 to Hagersten et al. in view of U.S. Pat. No. 6,185,658 B1 to Arimilli et al. as applied to claims 1,13 or 24 above, and further in view of U.S. Pat. No. 6,141,734 B1 to Razdan et al. Claims 9 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,887,138 to Hagersten et al. in view of U.S. Pat. No. 6,185,658 B1 to Arimilli et al. and further in view of U.S. Pat. No. 6,141,734 B1 to Razdan et al. as applied to claims 8 or 24 above, and further in view of U.S. Pat. No. 6,266,744 B1 to Hughes et al. These rejections are traversed.

Each of the independent claims recites one or more elements that are not taught or suggested in the art. These missing elements show that the differences between the combined teachings in the art and the recitations in the claims are great. As such, the pending claims are not a predictable variation of the art to one of ordinary skill in the art. Some examples are provided below with respect to claim 1.

As one example, independent claim 1 recites that the Owner processor begins write operations on said memory block and then displaces the exclusive copy of said memory block from said cache memory prior to completing the write operations on said memory block. The claim then recites that **in response to displacing said memory block prior to completing the write operations**, the Owner processor returns the displaced copy of said memory block to said Home processor with a signal indicating that said Owner processor remains a sharer of said memory block. The art does not teach or suggest these elements.

Hagersten teaches a multiprocessing computer system with processing nodes that determine whether an address of a memory transaction is a global or local address.

Hagersten also discusses different coherency states (modified, owned, shared, and invalid) employed by the computer system. Nowhere does Hagersten teach or suggest that a processing node displaces an exclusive copy of memory prior to completing write operations on the memory and then **in response to displacing the memory prior to completing such write operations** returns a signal indicating that the processing node remains a sharer of memory.

Arimilli teaches a method of evicting a cache block from a multi-processing computer system. After a cache miss, a cache block is selected for eviction based on a cache coherency state of the cache block. Nowhere does Arimilli teach or suggest that a processing node displaces an exclusive copy of memory prior to completing write operations on the memory and then **in response to displacing the memory prior to completing such write operations** returns a signal indicating that the processing node remains a sharer of memory.

The other cited art of record has at least the deficiencies that they do not teach or suggest a processing node displaces an exclusive copy of memory prior to completing write operations on the memory and then in response to displacing the memory prior to completing such write operations returns a signal indicating that the processing node remains a sharer of memory.

The differences between the claims and the teachings in the art are great since the cited references fail to teach or suggest all of the claim elements. As such, the pending claims are not a predictable variation of the art to one of ordinary skill in the art.

For at least these reasons, the claims are allowable over the cited art of record.

CONCLUSION

In view of the above, Applicants believe that all pending claims are in condition for allowance. Allowance of these claims is respectfully requested.

Any inquiry regarding this Amendment and Response should be directed to Philip S. Lyren at Telephone No. 832-236-5529. In addition, all correspondence should continue to be directed to the following address:

Hewlett-Packard Company
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Respectfully submitted,

/Philip S. Lyren #40,709/

Philip S. Lyren
Reg. No. 40,709
Ph: 832-236-5529